REMARKS

Claims 1-24 are pending.

Clams 18, 19, and 24 are amended to correct typographical errors.

The Applicants respectfully assert that the amendments to Claims 18, 19, and 24 and incorporated by reference in any claims depending therefrom, are not narrowing amendments made for a reason related to the statutory requirements for a patent that will give rise to prosecution history estoppel. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S. Ct. 1831, 1839-40, 62 U.S.P.Q.2d 1705, 1711-12 (2002); 234 F.3d 555, 566, 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2001).

I. EXAMINER INTERVIEW

The Applicants had a telephone interview with Examiner Kinkead on March 1, 2004. In the Examiner's interview, the Applicants' patent agent discussed the Examiner's reliance on the reference U.S. Patent No. 5,434,525 to *Leonowich* (hereafter "*Leonowich*") as the sole reference for rejecting Claims 1, 3, 4, and 7. The Applicants noted that in the first Office Action dated April 18, 2003, the Examiner stated that *Leonowich* "is silent on a selectable inverter circuit, and the reference Chow et al. is relied upon." In the present Office Action dated December 05, 2003, the Examiner now asserts the belief that *Leonowich* teaches the invention in Claim 1 of the present invention. The Applicants pointed out that Claim 1 recites three distinct elements, a ring oscillator circuit comprising a series connection of an odd number K of logic inverter gates wherein K is greater than three, a forward conduction circuit receiving control inputs, and a selectable inverter circuit receiving first and second mode control signals. While the Applicants agree that *Leonowich* does teach a ring oscillator circuit with three inverters and a forward conduction circuit receiving two variable voltages, the Applicants pointed out that *Leonowich* is silent on a selectable inverter circuit receiving first and second mode control signals and coupled in parallel with an Nth one of the K logic inverter gates. The

Examiner agreed that it appeared that *Leonowich* was in fact devoid of a selectable inverter circuit receiving first and second mode control signals and coupled in parallel with an Nth one of the K logic inverter gates. The Examiner recommended that the Applicants submit a response outlining Applicants' argument and he would consider it in light of our conversation. The Applicants further confirmed that the Examiner considered Claim 1 allowable if the limitations of Claim 2 were incorporated.

I. CLAIM OBJECTIONS

The Examiner objected to Claims 18 and 19 because of improper dependence. Claims 18 and 19 have been amended to properly depend from Claim 17. The Applicants also amended Claim 24 to properly depend from Claim 17.

II. REJECTION UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claims 1, 3, 4 and 7 under *35 U.S.C. § 103(a)* as being unpatentable over U.S. Patent No. 5,434,525 to *Leonowich* (hereafter "*Leonowich*"). The Examiner stated in the telephone interview of March 1, 2004 that the Applicants should repeat his arguments relative to *Leonowich* from the Office Action of April 18, 2003.

To establish a *prima facie* case of obviousness, the Examiner must meet three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be some reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim limitations.

A. Rejection of Claims 1, 3, 4 and 7.

Claim 1 recites a ring oscillator circuit comprising a series connection of an odd number K of logic inverter gates, wherein K is greater than three, a forward conduction circuit having a first input, a first output, and receiving control inputs, said forward

conduction circuit coupled in parallel with a selected sequence of logic inverter gates within said K logic inverter gates and a selectable inverter circuit, having a first inverter input, a first inverter output and receiving a first mode control signal and a second mode control signal, said first inverter input coupled to a logic input of an Nth logic inverter gate and said first inverter output coupled to a logic output of said Nth logic inverter gate, said Nth logic inverter gate selected from said K logic inverter gates, wherein a frequency range of said multi-mode VCO is selected in response to states of said first and second mode control signals.

Leonowich discloses a ring oscillator in FIG. 1 consisting of three inverters 11, and three forward conduction circuits 14, 15 receiving control voltages VCN and VCP. *Leonowich* does not teach or suggest the circuitry of FIG. 1 including a selectable inverter circuit receiving first and second mode control signals and coupled in parallel with one of the inverters of the ring oscillator path. The elements making up the forward conduction path cannot be both the forward conduction circuit and the selectable inverter. Claim 1 recites that the forward conduction path is coupled in parallel with a "selected sequence" of logic inverters gates within the K logic inverter gates making up the ring oscillator path. A forward conduction circuit of *Leonowich* is coupled in parallel with a single logic inverter and not a sequence of logic inverters as recited in Claim 1. If the forward conduction circuit of *Leonowich* is considered to be the "selectable inverter circuit" of Claim 1, then there is no additional circuit (receiving first and second mode control signals) that could be considered as the "selectable inverter circuit" recited in Claim 1. Therefore, the Applicants respectfully assert that the rejection of Claim 1 under *35 U.S.C. § 103(a)* as being unpatentable over *Leonowich* is traversed for the reasons stated above and pursuant to the Applicants' arguments in the telephone interview with the Examiner.

The Examiner appears to have only rejected Claims 3 and 7 in that they depend from rejected Claim 1. Likewise, Claim 4 appears to be rejected because it depends from rejected Claim 3. Therefore, the Applicants respectfully assert that the rejections of

Claims 3, 4, and 7 under *35 U.S.C. § 103(a)* as being unpatentable over *Leonowich* are traversed for the reasons stated above and pursuant to the Applicants' arguments in the telephone interview with the Examiner.

The Examiner has stated that Claims 2, 5, and 6 are allowable if they were rewritten in independent form. Claim 2 depends from Claim 1. The Applicants have traversed the rejection of Claim 1 and thus the Applicants respectfully assert that Claim 2 and Claims 5 and 6 which depend from Claim 2 are in condition for allowance.

Dependent Claim 8 was not addressed anew in the Office Action of December 05, 2003. Claim 8 depends from Claim 1 and the Applicants respectfully assert that any rejection of Claim 8 is traversed as the rejection of Claim 1 is traversed in the included arguments.

The Examiner has stated that Claims 9-24 are allowed and the Applicants thank the Examiner for allowing these claims.

III. CONCLUSION

Amending Claims 18, 19 and 24 as suggested by the Examiner overcomes the objections to these claims.

The rejections of Claims 1, 3, 4 and 7-8 under *35 U.S.C. § 103(a)* as being unpatentable over *Leonowich* are overcome. The rejections of Claims 2, 5, and 6 have been traversed as the rejection of Claim 1 has been traversed. Claims 9-24 are allowed.

The Applicants, therefore, respectfully assert that Claims 1-24 are now in condition for allowance and request an early allowance of these claims.

Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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